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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/002,696	10/31/2001	Eliyahou Harari	11587/M-12336 US	4652

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EXAMINER
WEISS, HOWARD

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 08/07/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/002,696	HARARI ET AL.
	Examiner	Art Unit
	Howard Weiss	2814

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 May 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *13,15-23 and 25-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *13,15-23 and 25-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 14 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Attorney's Docket Number: M-12336 US

Filing Date: 10/31/01

Continuing Data: RCE established 5/7/03

Claimed Foreign Priority Date: none

Applicant(s): Harari et al. (Samachisa, Yuan, Guterman)

Examiner: Howard Weiss

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 5/7/03 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 13, 15, 17, 18, 37, 38, 40 and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eitan (U.S. Patent No. 6,011,725) and Fazio (U.S. Patent No. 5,4440,505).

   Eitan shows most aspects of the instant invention (e.g. Figures 2 to 12) including:

   - programming means (Column 12 Line 60 to Column 13 Line 33) supplying voltages to the gates **24**, source **14** and drain **16** regions to one of two threshold levels in one of two defined portions **23** of a charge storage dielectric **18** containing silicon nitride
   - reading means for reading the programmed values as claimed (Column 13 Line 35 to Column 17 Line 30)

   Eitan does not show the storage of more then two defined ranges using hot-electron injection. Fazio et al. teach (e.g. Figures 3 and 4) to program memory cell arrays **22a** using at four (4) distinct levels of charge states **States 0-3** using hot-electron injection (Column 4 Lines 49 to 57) into a dielectric storage means (Column 4 Lines 2 to 6) to allow for rapid programming of multiple bits per single memory cell within a reasonable time period (Column 1 Lines 59 to 66) It would have been obvious to a person of ordinary skill in the art at the time of invention to program memory cell arrays using at four (4) distinct levels of charge states using hot-electron injection into a dielectric storage means as taught by Fazio et al. in the device of Eitan to allow for rapid programming of multiple bits per single memory cell within a reasonable time period.

4. Claims 16 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eitan and Fazio et al., as applied to Claim 13 above, and further in view of DiMaria (Journal de Physique 1981).

   Eitan and Fazio et al. show most aspects of the instant invention (Paragraph 3) except for the charge storage dielectric including silicon rich silicon dioxide. DiMaria

teaches (e.g. Figure 3) to use a charge storage dielectric including silicon rich silicon dioxide to produce a memory device with excellent breakdown characteristics (Page C4-1117 second paragraph). It would have been obvious to a person of ordinary skill in the art at the time of invention to use a charge storage dielectric including silicon rich silicon dioxide as taught by DiMaria in the device of Eitan and Fazio et al. to produce a memory device with excellent breakdown characteristics.

5. Claims 19, 21 to 26, 29 to 31 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ma et al. (U.S. Patent No. 5,278,439) and Fazio et al.

Ma et al. show most aspects of the instant invention (e.g. Figures 2 and 3) including:

- an array of memory cells **20**, **22** with elongated source and drain regions **20A**, **22A** within a substrate **26** and extending in a first direction and separated in a second direction perpendicular to said first direction
- a channel region **22** extending between said source/drain regions
- first and second conductive (control) gates **20C**, **22C** extending in said first direction and first and second storage elements **20B**, **22B**
- conductive word lines **28** extending in said second direction
- a third control transistor gate **24A** positioned between said storage elements and coupled by a gate dielectric to the channel **24G**

Ma et al. shows do not show the storage of more then two defined ranges using charge storage dielectric. Fazio et al. teach (e.g. Figures 3 and 4) to program memory cell arrays **22a** using at four (4) distinct levels of charge states **States 0-3** using hot-electron injection (Column 4 Lines 49 to 57) into a dielectric storage means (Column 4 Lines 2 to 6) to allow for rapid programming of multiple bits per single memory cell within a reasonable time period (Column 1 Lines 59 to 66) It would have been obvious to a person of ordinary skill in the art at the time of invention to program memory cell arrays using at four (4) distinct levels of charge states using hot-electron injection into a dielectric storage means as taught by Fazio

et al. in the device of Ma et al. to allow for rapid programming of multiple bits per single memory cell within a reasonable time period.

6. Claims 20 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ma et al. and Fazio et al., as applied to Claim 19 above, and further in view of Eckert et al. (U.S. Patent No. 5,889,303).

   Ma et al. and Fazio et al. show most aspects of the instant invention (Paragraph 5) except for the charge trapping material extending continuously between two control gates. Eckert et al. teach (e.g. Figures 10 and 11) to have charge storage material **106** extend between two control gates **110a,b** to reduce gate oxide stress (Column 2 Lines 37 to 60). It would have been obvious to a person of ordinary skill in the art at the time of invention to have charge storage material extend between two control gates as taught by Eckert et al. in the device of Ma et al. and Fazio et al. to reduce gate oxide stress.

7. Claims 27, 32 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ma et al. and Fazio et al., as applied to Claim 19 above, and further in view of Aritome et al. (IEDM 95).

   Ma et al. and Fazio et al. show most aspects of the instant invention (Paragraph 5) except for the word lines recessed into the substrate. Aritome et al. teach (e.g. Figure 1) to recess word lines into the substrate to realize a very low bit cost (see Abstract). It would have been obvious to a person of ordinary skill in the art at the time of invention to recess word lines into the substrate as taught by Aritome et al. in the device of Ma et al. and Fazio et al. to realize a very low bit cost.

8. Claims 34 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ma et al. (U.S. Patent No. 6,346,725 and hereinafter Ma '725) and Fazio et al.

Ma '725 show most aspects of the instant invention (e.g. Figures 3) including:

- an array of memory cells **S1** to **S6** with elongated source **120** and drain **30** regions within a substrate **40** and extending in a first direction and separated in a second direction perpendicular to said first direction
- a channel region **80** extending between said source/drain regions
- conductive control lines **70** extending in said first direction and adjacent one of said source/drain regions in a first portion of space between said regions
- conductive word lines **710** spaced apart in said first direction, extending in said second direction over said control lines and positioned over a second portion of space neighboring source/drain regions
- charge storage material **60** position between said word and control lines

Ma '725 shows do not show the storage of more then two defined ranges using dielectric charge storage material and the explicit programming and reading circuits. Fazio et al. teach (e.g. Figures 3 and 4) to program memory cell arrays **22a** using at four (4) distinct levels of charge states **States 0-3** using hot-electron injection (Column 4 Lines 49 to 57) into a dielectric storage means (Column 4 Lines 2 to 6) to allow for rapid programming of multiple bits per single memory cell within a reasonable time period (Column 1 Lines 59 to 66) It would have been obvious to a person of ordinary skill in the art at the time of invention to program memory cell arrays using at four (4) distinct levels of charge states using hot-electron injection into a dielectric storage means as taught by Fazio et al. in the device of Ma et al. to allow for rapid programming of multiple bits per single memory cell within a reasonable time period.

9. Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ma '725 and Fazio et al., as applied to Claim 19 above, and further in view of Eckert et al.

Ma '725 and Fazio et al. show most aspects of the instant invention (Paragraph 8) except for the charge trapping material extending continuously between two control

gates. Eckert et al. teach (e.g. Figures 10 and 11) to have charge storage material **106** extend between two control gates **110a,b** to reduce gate oxide stress (Column 2 Lines 37 to 60). It would have been obvious to a person of ordinary skill in the art at the time of invention to have charge storage material extend between two control gates as taught by Eckert et al. in the device of Ma '725 and Fazio et al. to reduce gate oxide stress.

Response to Arguments

10. The Applicants' arguments with respect to Claims 13, 15 to 23 and 25 to 41 have been considered but are moot in view of the new ground(s) of rejection. In reference to the claims rejected using Ma et al., said claims do not state that the charge storage is in a conductive or dielectric material.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Wada et al. (U.S. Patent No. 5,424,978) teach to program multiple charge levels using hot-electron injection.

12. Papers related to this application may be submitted directly to Art Unit 2814 by facsimile transmission. Papers should be faxed to Art Unit 2814 via the Art Unit 2814 Fax Center located in Crystal Plaza 4, room 3C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2814 Fax Center number is **(703) 308-7722** or **-7724**. The Art Unit 2814 Fax Center is to be used only for papers related to Art Unit 2814 applications. The official TC2800 Before-Final, **(703) 872-9318,** and After-Final, **(703) 872-9319**, Fax numbers will provide the fax sender with an auto-reply fax verifying receipt of their fax by the USPTO.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Howard Weiss at **(703) 308-4840** and between the

hours of 8:00 AM to 4:00 PM (Eastern Standard Time) Monday through Friday or by e-mail via **Howard.Weiss@uspto.gov**.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group 2800 Receptionist at **(703) 308-0956**.

14. The following list is the Examiner's field of search for the present Office Action:

Field of Search	Date
U.S. Class / Subclass(es): 257/ 324, 326	thru 7/23/03
Other Documentation: none	
Electronic Database(s): EAST, IEL	thru 7/23/03

HW/hw
23 July 2003

Howard Weiss
Examiner
Art Unit 2814